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PUB-NO: JP401315856A
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TITLE: SLAVE BOARD PRESENCE/ABSENCE RECOGNIZING SYSTEM

PUBN-DATE: December 20, 1989

INVENTOR-INFORMATION:

NAME	COUNTRY
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ABSTRACT:

PURPOSE: To prevent a system down due to the error of the bus time out or the error of address setting from being generated by receiving a signal generated by means of a response signal generating part as a response signal, and recognizing the presence and absence of a slave board by means of the presence and absence of the reception of an interrupting signal.

CONSTITUTION: An interrupting signal output part 212 decodes an address from a host CPU 11, compares data obtained from a data bus with reference data to discriminate a self-board 20, and at the time of coincidence, the part 212 sends an interrupting signal IRQ to a system bus 100. Further, the host CPU 11 of a CPU board 10 sends the address to designate the slave board 20, first receives a response signal ACK generated by a response signal generating part 12, then, receives the interrupting signal IRQ by the interrupting signal output part 212 of the slave board 20, and the existence of the designated slave board 20 is recognized. Thus, the system down due to the error caused by the bus time out or the error of the switch setting can be prevented from being generated.